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Reversible Multiplier with Peres Gate and Full Adder.

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Abstract: *Low Power dissipation and smaller area are one of the important factors while designing multipliers for digital circuits. As multipliers used in digital circuits dissipate large amount of heat whenever there is a transition of bits. Reversible Logic has emerged as a promising technology in reducing power dissipation. It has application in various fields such as low power VLSI, Quantum computing and Nano-technology. Hence, In this paper we try to design a reversible multiplier using Peres gate and Full adder. We show that, proposed multiplier is efficient in terms area, power and delay. Furthermore, it requires fewer garbage outputs and constant inputs. Proposed reversible multiplier is implemented using VHDL, simulated and synthesized on Xilinx 13.1 tool.*

Keywords: *Constant input, Digital circuits, Full adder, Garbage output, Multipliers, Reversible Logic, Peres gate. VHDL, Xilinx.*

I. Introduction

Multiplication is heavily used algorithm in many computational units. It is vital for processors to have low power multipliers. Multipliers play an important role in many high performance systems such as Microprocessors, Digital Signal Processing, Fir filters etc. Performance of any system is generally determined by the performance of multiplication unit. Because multiplication is a most power consuming and slowest process in any computational unit. Hence designing a efficient multiplier in terms of area, power and delay is a major objective in this work.

Multipliers designed with reversible logic are one of the best solution to reduce power dissipation. As demonstrated by R.Landauer in the early 1960, irreversible hardware computation regardless of its realization technique, results in energy dissipation due to the information loss [1].It is proved that the loss of each one bit of information dissipates at least KTln2 joules of energy (heat), where K=Boltzmann's constant and T=absolute temperature at which operation is performed[1]. In .1973, Bennet showed that in order to avoid KTln2 joules of energy dissipation in a circuit, it must be built using reversible logic gates [2]. In this paper we try to design a reversible multiplier with Peres gate and Full adder.

II. Basic Definitions Related To Reversible Logic

An n input n output function is said to be reversible if there is one to one correspondence (mapping) between inputs and outputs. Hence, in any reversible system number of inputs is always equal to number of outputs. Also the input vector can always be determined from its output vector [4-6]

A) **Reversible Function** :

A multiple output Boolean function (x1: x2: xn) of n Boolean variables is called as reversible if

1) The number of outputs is equal to number of inputs.
2) If reversible function performs permutations of set of input vectors.

B) **Reversible Logic Gate** :

Reversible Logic gates are circuits in which number of inputs is equal to number of outputs and there is one to one mapping between inputs and outputs[3-5].It not only helps us to determine output vectors from input vectors but also we can uniquely determine input vectors from its output vectors[4-6].

C) **Constant Inputs** :

This refers to number of inputs that has to be maintained constant at 1 or 0 in order to synthesize the given logical function [7].

D) **Garbage Outputs** :

The output that is added to an n x k function to make it reversible is called as garbage output[6].

The following simple formula shows the relation between constant inputs and garbage outputs :

(Input + Constant inputs) = (Output + Garbage Outputs).

E) **Quantum Cost** :

Quantum cost refers to the cost of the circuit in terms of the cost of primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of a circuit is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1*1 gate is 0 and that of 2*2 gates is unity [8].

F) **Flexibility** :

Flexibility refers to the universal nature of a reversible logic gate in realizing more functions [9].

G) **Gate Level** :

It refers to number of levels required to realize the given function.

H) **Hardware Complexity** :

This refers to total number of logic operations in a circuit, i.e. total number of AND,OR EXOR operations in a circuit[10-11].

I) **Design Constraints for Reversible Logic Circuits** :

The following are the important design constraints for reversible logic circuits:

a) Reversible Logic circuits do not allow fan-outs.
b) Should use minimum number of constant inputs.
c) Should use minimum number of garbage outputs.
d) Should use minimum gate levels or logic depth.
e) Should have minimum quantum cost.

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III. Reversible Logic Gates

There are many number of reversible logic gates that exist at present. The quantum cost of each reversible logic gate is an important optimization parameter [12]. The quantum cost of a 1x1 reversible gate is assumed to be zero while the quantum cost of a 2x2 reversible logic gate is taken as unity. The quantum cost of other reversible gates is calculated by counting the number of V, V+ and CNOT gates present in their circuit. V is the square root of NOT gate and V+ is its Hermit an.

An n x n reversible gate can be represented as:

Iv = (I1, I2, I3…In)
Ov = (O1, O2, O3….On)

Where Iv and Ov are input and output vectors respectively.

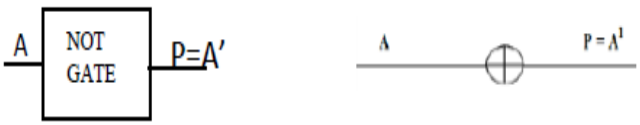
The V and V+ quantum gates have the following properties:

V * V = NOT ……. (1)
V * V+ = V+ * V = 1 ……. (2)
V+ * V+ = NOT ……. (3)

Some of the important reversible logic gates are,

1) **NOT Gate**

The simplest Reversible gate is NOT gate and is a 1*1 gate [13]. The Reversible 1*1 gate is NOT Gate with zero Quantum Cost is as shown in the Figure 1.



(a) Block diagram (b) symbol

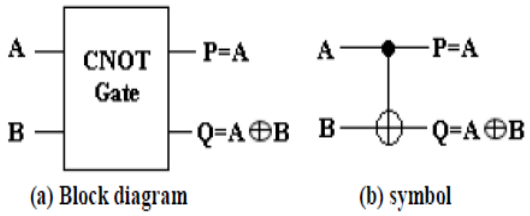
Figure1. NOT gate

2) **CNOT GATE**

CNOT gate is also known as controlled-not gate. It is a 2*2 reversible gate. The CNOT gate can be described as:

Iv = (A, B) ; Ov = (P= A, Q= A B)

Iv and Ov are input and output vectors respectively. Quantum cost of CNOT gate is 1[14]. Figure 2 shows a 2*2 CNOT gate and its symbol.

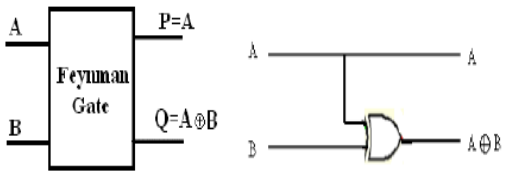


(a) Block diagram (b) symbol

Figure 2: CNOT Gate

3) **FEYNMAN Gate**

The Feynman gate which is a 2*2 gate and is also called as Controlled NOT and it is widely used for fan-out purposes. The inputs (A, B) and outputs P=A, Q= A XOR B. It has Quantum cost one [15]



(a) Block diagram (b) Logic circuit

Figure 3: FEYNMAN Gate

4) **Double Feynman Gate (F2G**)

It is a 3*3 Double Feynman gate [16].The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q=AÅB, R=AÅC. Quantum cost of Double Feynman gate is 2.

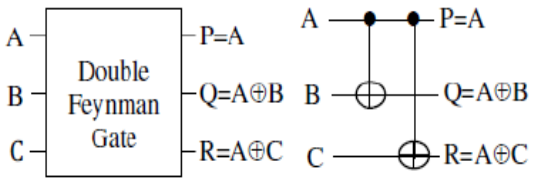
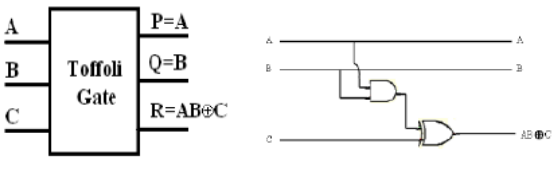


Figure 4: Double Feynman gate.

5) **TOFFOLI Gate:**

TOFFOLI gate which is a 3*3 gate with inputs (A, B, C) and outputs P=A,Q=B, R=AB XOR C. It has Quantum cost five [17].

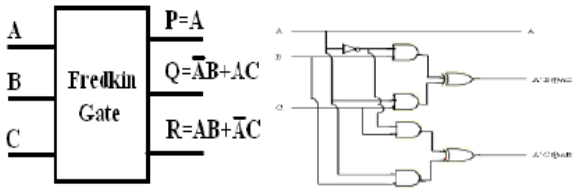


(a) Block diagram (b) Logic circuit

Figure 5: Toffoli Gate

6) **FREDKIN Gate:**

Fredkin gate which is a 3*3 gate with inputs (A, B, C) and outputs P=A, Q=A'B+AC, R=AB+A'C. It has Quantum cost five [18].

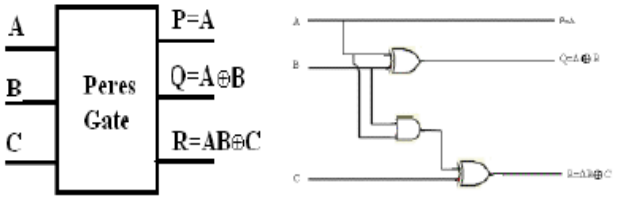


(a) Block diagram (b) Logic circuit

Figure 6: Fredkin Gate

7) **PERES Gate:**

Peres gate which is a 3*3 gate having inputs (A, B, C) and outputs P = A; Q = A XOR B; R = AB XOR C. It has Quantum cost four [19].



(a) Block diagram (b) Logic circuit

Figure 7: Peres Gate

IV. Proposed Reversible Multiplier

General multiplier is basically based on two steps:

a) Generation of partial products

b) Addition of partial products.

Partial Product Generation				x	x_3 y_3	x_2 y_2	x_1 y_1	x_0 y_0
					x_3y_0	x_2y_0	x_1y_0	x_0y_0
				x_3y_1	x_2y_1	x_1y_1	x_0y_1	
Multi Operand Addition			x_3y_2	x_2y_2	x_1y_2	x_0y_2		
		x_3y_3	x_2y_3	x_1y_3	x_0y_3			
	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

The operation of the partial products can be generated in parallel using 16 Peres gates as shown in Fig.8 because of lower hardware complexity, we use Peres gate instead of other reversible gates. This structure is proposed in [20].

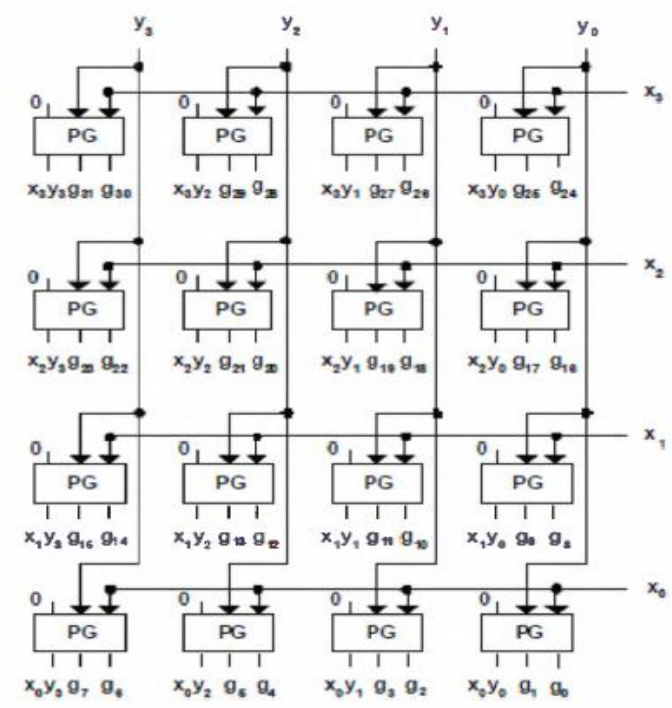


Fig.8 Partial Products Generation (PPG) using Peres gate

The purpose of this paper is the design of reversible multiplier using VHDL, with the aim of optimizing its hardware complexity to make it more economical in terms of number of garbage Therefore we have used a Full adder having zero garbage outputs and zero constant inputs. The proposed full adder will be of great help in reducing the garbage outputs and constant input parameters.

Output variable Sum in a Full Adder can be implemented using simple XOR gates as shown in fig 9.

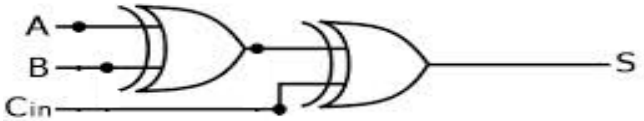


Fig.9 Gate Implementation of SUM in Full Adder.

The carry of the next stage in Full Adder can be expressed as:

$Q = \overline{(\overline{AB})\ (\overline{BC})\ (\overline{AC})}$ as shown in fig 10.

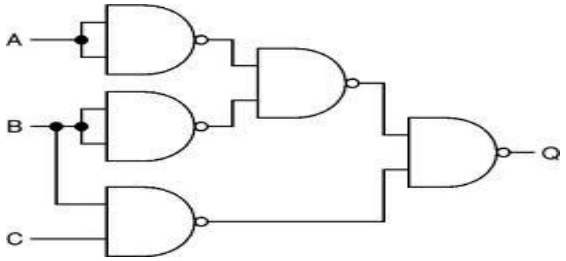


Fig.10 Gate Implementation of Output Carry in Full Adder.

NAND gates are used for faster carry propagation and help us to improve speed.

Proposed reversible uses eight full adders that they produce zero garbage outputs and zero constant inputs. In addition, it needs four reversible adders. We use Peres gate as reversible half adder, because it has less hardware complexity. Addition of partial products requires 8 full adders and 4 half adders as shown in fig 11

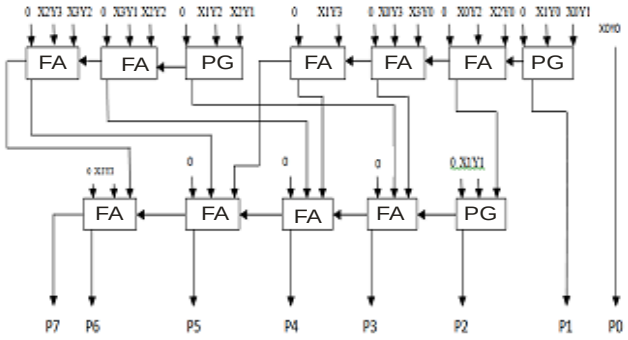


Fig.11 Reversible multiplier architecture (4bit) where outputs of PPG are input of full adder and Peres gate (half adder)

Proposed 4 bit reversible multiplier can be generalized for 8 bit and higher order multiplication using following algorithm (fig 12) .

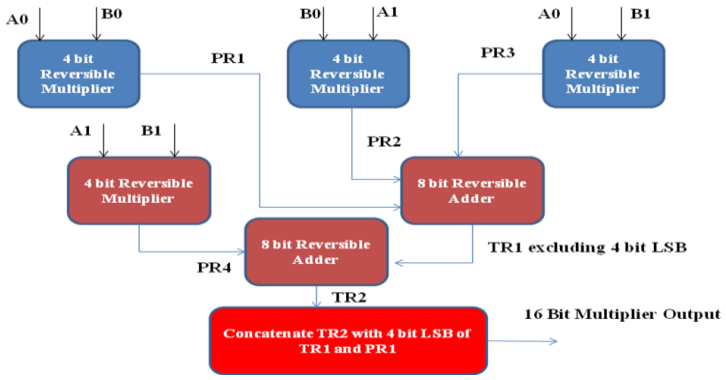


Fig.12 8 bit multiplier using 4 bit multiplier.

V. Results.

Complete code of reversible multiplier (4bit, 8bit and 16bit) is
Written using VHDL, simulated using Xilinx ISE 13.1
Simulator and synthesized using Xilinx synthesis tool (XST)
13.1. Power analysis performed using Xilinx X Power
Analyzer. Target FPGA used belongs to SPARTAN 3 families, XC3S50 device, VQ100 package, speed grade - 5.
Fig. 13, 14, 15 shows the simulation results, device utilization
Summary and power analysis respectively.

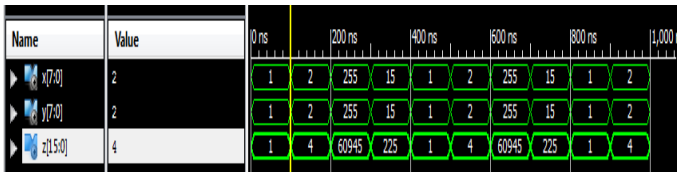
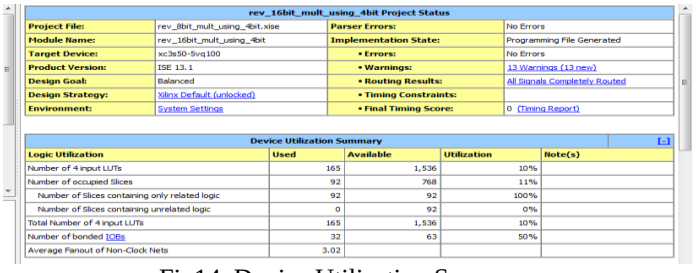


Fig13.Simulation Results



rev_16bit_mult_using_4bit Project Status

Project File:	rev_8bit_mult_using_4bit.xise	Parser Errors:	No Errors
Module Name:	rev_16bit_mult_using_4bit	Implementation State:	Programming File Generated
Target Device:	xc3s50-5vq100	• Errors:	No Errors
Product Version:	ISE 13.1	• Warnings:	13 Warnings (13 new)
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	0 (Timing Report)

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	165	1,536	10%	
Number of occupied Slices	92	768	11%	
Number of Slices containing only related logic	92	92	100%	
Number of Slices containing unrelated logic	0	92	0%	
Total Number of 4 input LUTs	165	1,536	10%	
Number of bonded IOBs	32	63	50%	
Average Fanout of Non-Clock Nets	3.02			

Fig14. Device Utilization Summary

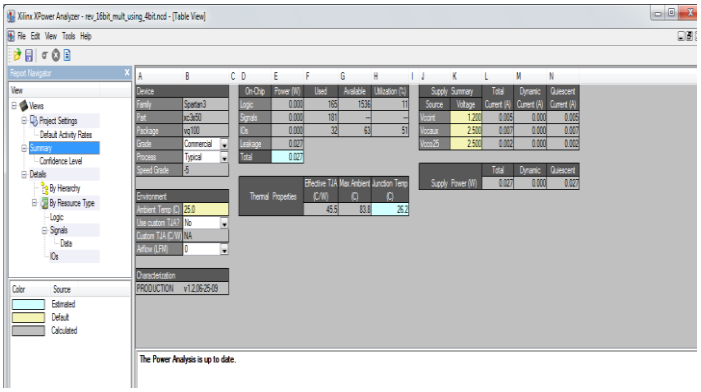


Fig15. Power Analysis

Table 1: Results of 4bit, 8bit and 16bit reversible multipliers.					
Parameter	**Delay**	**Power**	**Slices Used**	**4 Input LUT**	**Bonded IOBs**
4 Bit	13.65ns	16mw	18	29	16
8 Bit	29.23ns	29mw	95	165	32
16 Bit	42.45ns	38.20mw	127	254	46.25
Table 2: Comparison of Reversible and Conventional Multipliers.					
Parameter	**Delay**	**Power**	**Slices Used**	**4 Input LUT**	**Bonded IOBs**
4 Bit Rev. Multiplier	13.65ns	16mw	18	29	16
4 Bit Conv. Multiplier	16.32ns	27mw	18	32	16

Table 3: Comparison of different 4bit reversible multipliers						
Paper No.	**NoG**	**Gout**	**Gin**	**QC**	**No. of Logical Calculations**	**CC**
This Work	28	20	20	80	16×(2a+1b)(for PG)+ 8×(2a+5b+5c) (for PFAG)+4×(2a+1b) (for PG)	56a + 60b +40c
[21] First Design	28	28	28	128	16×(2a+1b)(for PG)+ 8×(5a+2b) (for PFAG)+4×(2a+1b) (for PG)	80a+36b
[21] Second Design	28	28	28	153	9×(1a+1b)(for TG)+7×(2a+1b)(for PG)+8×(5a+ 2b)(for PFAG)+4× (2a+1b) (for PG)	71a+36b
[22]	28	28	28	137	9×(1a+1b)(for TG)+7 × (2a+1b)(for PG)+8× (5a+2b)(for HNG)+4× (2a+1b)(for PG)	71a+36b
[23]	44	52	44	160	(80+16)a+36b	96a+36b
[24]	44	52	44	160	(80+16)a+36b	96a+36b
[25]	44	56	48	236	(92+16)a+52b+36d	108a+52b+36d
[26]	45	58	50	278	(110+16)a+103b+71d	126a+103b+71d
[27]	56	56	47	220	(80+16)a+100b+68d	96a+100b+68d

We define:
a=A two input XOR calculation.
b=A two input AND gate calculation.
c=A NOT gate calculation.
NoG = Number of Logic Gates.
Gout = Number of Garbage outputs.
Gin = Number of Garbage Inputs.
QC = Quantum Cost.
CC = Circuit Cost.

As shown in table3, our proposed design requires only 28 reversible gates and is also optimized in terms of number of garbage outputs, number of constant inputs and hardware complexity.

VI. Conclusion.

Table 2 shows that proposed reversible multiplier using Peres gate and Full Adder is better in terms of area power and delay as compared with conventional multiplier. Furthermore, Table 3 shows that it is efficient in terms of number of garbage outputs, constant inputs and quantum cost as compared with other reversible multipliers. However, we need synthesizing methods to minimize number of garbage outputs and constant inputs. We are short of simulation, synthesis, testing and verifying tools for designing reversible logic. But researchers around the world have been doing exciting research and making progress in this direction. Soon, reversible computing will become promising technology in near future.

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